REMARKS

The Applicant thanks the Examiner for the thorough examination of the application. No new matter is believed to be added to the application by this Amendment.

Entry of Reply

Entry of this Reply under 37 C.F.R. §1.116 is respectfully requested because it places the application into allowance. Alternately, entry of this Reply is respectfully requested because it places the application because it places the application in better form for appeal.

Claims 1 and 11 have been amended in this Reply. However, these amendments do not raise any new issues because the amendments address issues that were already raised by the Examiner in Paragraph 5 at page 6 of the Office Action.

Status of the Claims

Claims 1-16 are pending in the application. The amendments to the claims find support in *inter alia* Figure 4 of the application.

Rejection Under 35 U.S.C. §103(a) Over Uchino and Nakano (and Itakura)

Claims 1, 3-5, 7-9 and 11-16 are rejected under 35 U.S.C. §103(a) as being obvious over Uchino (U.S. Patent 6,040,816) in view of Nakano (U.S. Patent 6,529,181). The Examiner adds the teachings of Itakura (U.S. Patent 5,252,957) to reject claims 2, 6 and 10. Applicant traverses.

The Present Invention and its Advantages

The present invention pertains to a novel LCD device that increases display quality by minimizing EMI (electromagnetic interference). The inventive LCD device utilizes a synchronized data sampling technology and timing controller configuration that minimizes the use of unnecessary voltage, thereby decreasing power consumption.

The present invention finds a typical embodiment in instantly amended claim 1, which sets forth:

> 1. An LCD device, comprising:
> a LCD panel;
> a plurality of source drivers applying data signals to the LCD panel;
> a plurality of gate drivers applying gate driving signals to the LCD panel;
> a timing controller outputting to the source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each output signal to the source drivers; and
> at least two data buses transmitting the data separately output from the timing controller to the source drivers.

As shown in Figure 4, source drivers 43 apply data signals to the LCD panel 41, and the gate drivers 45 apply gate-driving signals to the LCD panel 41. The timing controller 47 receives a data clock signal DCLK and R/G/B digital data, and outputs first and second clock signals CLK1 and CLK2 having different phases and various control signals to control the source and gate drivers 43 and 45. The timing controller 47 connects to each source driver by a first data bus DB1 transmitting the digital data synchronized with the first clock signal CLK1 to each source driver 43, and a second data bus DB2 transmitting the digital data synchronized with the second clock signal CLK2 to each source driver 43.

Instant claims 1 and 11 better elucidate the relationship of the timing controller to the LCD device.

Distinctions of the Invention over Uchino, Nakano and Itakura

Distinctions of the invention over the prior art have been place before the Examiner in the Reply filed January 6, 2004. For brevity, these distinctions are not repeated here.

The Examiner admits to many of the failings of Uchino. At page 3 of the Office Action, the Examiner admits that "Uchino fails to specifically teach that the clock signals are input to the source drivers from a timing controller. . ." The Examiner also admits to further failures of Uchino, stating: "Uchino also fails to specifically teach the usage of two data buses transmitting data from the external device to the drivers." The Examiner further admits that "With reference

to claims 11 and 16, Uchino also fails to teach that the data synchronized with the respective clock signal for each odd/even numbered or R/G/B/ data through different data busses."

The invention, in contrast, shows a fundamentally different driving logic. As shown in Figure 4 of the invention, the timing controller 47 feeds both clock signals CLK1, CLK2 and RGB data to source drivers 23. The timing controller 23, provides the logic comparable to what the logical circuits 70a, 70b, 70c . . . of Uchino provide, but at a fundamentally different location in the circuit.

The Examiner then turns to Fig. 1 of Nakano and tries to graft a fundamentally different circuit logic onto that of Uchino.

In his response to arguments in paragraph 5 at page 6 of the Office Action, the examiner acknowledges the failings of Uchino, but states:

> Also, the claims do not recite that the timing controller (47) feeds clock signals as sell as image data to the source driver as argued by the applicant. Therefore, the arguments made about the positioning of the control circuit of Nakano, which operates as the timing controller, being different in location to the logical circuits of Uchino is irrelevant.

However, claim 1 has been amended to more clearly set forth the function of the timing controller, stating: "a timing controller outputting to the source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each output signal to the source

drivers. . ." Independent claim 11 has also been amended to better elucidate the timing controller.

As a result, a person having ordinary skill in the art could not combine Uchino and Nakano to produce the invention as embodied in instant independent claims 1 and 11. A *prima facie* case of obviousness has thus not been made over Uchino and Nakano. Claims dependent upon claims 1 and 11 are patentable for at least the above reasons.

The Examiner turns to Itakura to reject dependent claims 2, 6 and 10. Itakura, however, fails to address the deficiencies of Uchino and Nakano.

These rejections are accordingly overcome and withdrawal thereof is respectfully requested.

Prior Art Cited But Not Utilized By The Examiner

The prior art cited but not utilized by the Examiner shows the status of the conventional art that the invention supercedes. No additional remarks are accordingly necessary.

Priority

The Examiner has acknowledged priority most recently in the Office Action Summary of the Office Action mailed March 22, 2004.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E. Goozner (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By Robert E Goozner #42,593
for Joseph A. Kolasch, #22,463

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

JAK/REG/jls/bsh
0465-0883P

(Rev. 09/30/03)